<WHAT IS CLAIMED IS:>

1. A bias voltage generating circuit, comprising:

a driving unit which generates a bias voltage to be applied to a predetermined load; and

a control unit which switches a current driving capability of the driving unit according to a variation in an amount of current required for the load in a period for applying the bias voltage to the load.

2. The bias voltage generating circuit according to claim 1, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have different current driving capabilities, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

3. The bias voltage generating circuit according to claim 1, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have the same current driving capability, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

4. The bias voltage generating circuit according to claim

1, wherein

the predetermined load is an amplifier which is included in an AD converter.

5. The bias voltage generating circuit according to claim 2, wherein

each of the plurality of bias circuits includes:

a CMOS transistor composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage;

a switching element which interrupts a feedthrough current occurring from the CMOS transistor; and

a switching element which controls output of the bias voltage from the CMOS transistor.

6. The bias voltage generating circuit according to claim 3, wherein

each of the plurality of bias circuits includes:

a CMOS transistor composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage;

a switching element which interrupts a feedthrough current occurring from the CMOS transistor; and

a switching element which controls output of the bias voltage from the CMOS transistor.

7. The bias voltage generating circuit according to claim 5, wherein

the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits.

8. The bias voltage generating circuit according to claim 6, wherein

the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits.

9. The bias voltage generating circuit according to claim 1, wherein

the driving unit includes a bias circuit which can output a first bias voltage and a second bias voltage which are different from each other, selectively; and

the control unit switches the output of the driving unit between the first bias voltage and the second bias voltage according to a variation in the amount of current necessary for the load.

10. The bias voltage generating circuit according to claim 9, wherein

the bias circuit is a Wilson type current mirror circuit which includes at least a pair of n-channel transistors having

different size ratios, a pair of p-channel transistors having generally the same size ratios, and a switching element which switches the output between the first bias voltage and the second bias voltage.

11. An amplifier circuit, comprising:

an amplifier unit which repeats an auto-zero operation and an amplification operation alternately;

a driving unit which supplies the amplifier unit with a bias voltage; and

a control unit which switches the current driving capability of the driving unit according to a variation in an amount of current required between the auto-zero operation and the amplification operation of the amplifier unit.

12. The amplifier circuit according to claim 11, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have different current driving capabilities, and

the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits.

13. The amplifier circuit according to claim 11, wherein

the driving unit includes a plurality of bias circuits which are connected in parallel and have the same current driving capability, and

the control unit switches the current driving capability

by controlling the number of circuits to operate out of the plurality of bias circuits.

14. The amplifier circuit according to claim 12, wherein each of the plurality of bias circuits includes:

a CMOS transistor composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage;

a switching element which interrupts a feedthrough current occurring from the CMOS transistor; and

a switching element which controls output of the bias voltage from the CMOS transistor.

15. The amplifier circuit according to claim 13, wherein each of the plurality of bias circuits includes:

a CMOS transistor composed of a PMOS transistor and an NMOS transistor which are connected in series between a power supply potential and a ground potential and have a common drain connected to their respective gates, the drain outputting the bias voltage;

a switching element which interrupts a feedthrough current occurring from the CMOS transistor; and

a switching element which controls output of the bias voltage from the CMOS transistor.

16. The amplifier circuit according to claim 14, wherein

the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits.

17. The amplifier circuit according to claim 15, wherein the control unit controls the number of circuits to operate by sending control signals to the respective switching elements included in the plurality of bias circuits.

18. The amplifier circuit according to claim 11, wherein the driving unit includes a bias circuit which can output a first bias voltage and a second bias voltage which are different from each other, selectively; and

the control unit switches the output of the driving unit between the first bias voltage and the second bias voltage according to a variation in the amount of current necessary for the load.

19. The amplifier circuit according to claim 18, wherein the bias circuit is a Wilson type current mirror circuit which includes at least a pair of n-channel transistors having different size ratios, a pair of p-channel transistors having generally the same size ratios, and a switching element which switches the output between the first bias voltage and the second bias voltage.

20. A pipelined AD converter having a plurality of stages of conversion units which generate several bits of digital values of descending order from an input analog voltage,

respectively, the AD converter comprising:

an amplifier unit which repeats an auto-zero operation and an amplification operation alternately;

a driving unit which supplies the amplifier unit with a bias voltage; and

a control unit which switches a current driving power of the driving unit according to a variation in the amount of current required between the auto-zero operation and the amplification operation of the amplifier unit,

the control unit controlling the current driving capability so as to drive at least any one of the plurality of stages of conversion units with a relatively high current and drive the other conversion units with a lower current.

21. The pipelined AD converter according to claim 20, wherein

the control unit controls the current driving capability so as to drive the conversion unit at the initial stage with a relatively high current and drive the second and subsequent conversion units with a lower current.